REMARKS IN REGARD TO CLAIM REJECTIONS - 35 USC § 112

Applicants thank the Examiner for pointing out the correction needed to claims 6-8. As applicant has clearly provided in the specification, different species will be used for the sidewall implant depending on whether N-channel MOS transistors or P-Channel MOS transistors are being formed.

REMARKS IN REGARD TO CLAIM REJECTIONS - 35 USC § 102

The Examiner rejected claims 5-7 under 35 U.S.C. § 102(b) as being anticipated by Mehta, et al. (U. S. Patent No. 5,646,063). Applicants respectfully disagree.

Mehta does not disclose a method for fabricating a shallow-trench isolation transistor in a single isolation trench having a uniform cross section to define an active region in the silicon substrate as shown and disclosed in Applicants' invention.

Mehta teaches using different trench sizes to form narrow active areas and wide active areas. NMOS devices face the problem of the reverse narrow width effect in the shallow trench isolation process. The reverse narrow width effect problem increases the sub-threshold leakage. Mehta attempts to solve this problem by forming trenches of different sizes. The different size trenches can be processed differently. Mehta teaches using an implant in one trench and not the other in order for the two trenches to be isolated from each other.

Applicants teach a shallow trench isolation transistor having a uniform cross section of annular length. Claim 5 as amended.

Mehta does not teach a transistor bounded by isolation trenches having a uniform cross section of annular length. In fact, Mehta teaches a transistor separated by a trench isolation region 134, and a wide isolation region 141 similar to isolation region

130. Mehta, column 6, lines 38 through 49. Mehta does not teach a transistor having a uniform cross section of annular length. Thus, Mehta does not teach all the claim limitations as required under 35 U.S.C. 102(b).

If a prior art reference cited as anticipating a claimed invention is shown to lack a characteristic of the claimed invention, that proof negates the assertion that the claimed invention was described in the prior art. *In re Mills*, 16 USPQ 2d 1430, 1432 (Fed. Cir. 1990). Thus, Applicants' claims 5-8 are not anticipated by Sample.

REMARKS IN REGARD TO CLAIM REJECTIONS - 35 USC § 103

The Examiner has rejected claim 8 as being unpatentable under 35 U.S.C. 103(a) over Mehta as applied to claim 5 above, and further in view of Liaw, et al. (U.S. Patent No. 5,960,276). Applicants respectfully disagree.

As set forth above, Mehta does not teach all the claim limitations. In addition, Mehta actually teaches away from the claimed invention by teaching that the isolation trenches must be of varying width. Teaching away is the antithesis of the art suggesting that the person of ordinary skill go in the claimed direction. *In re Fine,* 837 F.2d 1071, 5 U.S.P.Q. 2d 1596 (Fed. Cir. 1988). Claim 6 is neither anticipated nor obvious. Therefore, if an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. *Id.*

CONCLUSION

For the foregoing reasons, Applicants submit that all of the claims elected in this application, claims 5-8, are in condition for allowance and Applicants respectfully request reexamination of the present application, reconsideration and withdrawal of the

present rejections. Should there be any further matter requiring consideration, the Examiner is invited to contact the undersigned counsel.

For these reasons, and in view of the above amendments, this application is now considered to be in condition for allowance and such action is earnestly solicited.

Respectfully Submitted,
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Dated: 8/28/02

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APPENDIX A: MARKED-UP SPECIFICATION

In The Claims

Kindly amend claims 5 through 8 as follows:

5. (Amended) A method for fabricating a shallow-trench isolation transistor on a semi-conductor substrate including:

forming [an] a single isolation trench having a uniform cross section to define an active region in the silicon substrate;

performing sidewall isolation implants on the side and bottom walls of said isolation trench;

depositing a dielectric isolation material in said isolation trench;

planarizing the top surface of said silicon substrate and said dielectric isolation material;

forming a gate oxide layer over said active region in said silicon substrate;

forming and defining gate regions over said oxide layer in said active region in said silicon substrate; and

forming source and drain regions in the active region in the silicon substrate.

6. (Amended) The method of claim 5 wherein performing said sidewall implants comprises implanting [n-type] p-type impurities.

7. (Amended) The method of claim 6 wherein implanting [n-type] p-type impurities comprises implanting boron.

8. (Amended) The method of claim 6 wherein implanting [n-type] p-type impurities comprises implanting boron to a concentration of about 2e12.